REMARKS

Claim 26-31 have been amended. Claims 35-46 have been added. Claims 1-25 and 32-34 have been canceled. Claims 26-31 and 35-46 are pending. The specification has been amended. Applicant reserves the right to pursue the original claims and other claims in this and other applications.

Affirmation of Election

During a telephone conversation with the Examiner on June 25, 2007, Applicant's representative made a provisional election without traverse to prosecute Group II (claims 26-31). That election is hereby affirmed.

35 U.S.C. § 101 Rejections

Claims 26-31 stand rejected under 35 U.S.C. § 101 as being directed to non-statutory subject matter. Claims 26-31 have been amended to recite a "digital circuit" in response to this rejection. Accordingly, the rejection should be withdrawn and the claims allowed.

35 U.S.C. § 103(a) Rejections

Claims 26-31 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent 6,038,582 (Arakawa) in view of U.S. Patent 5,359,548 (Yoshizawa). Applicant respectfully traverses these rejections.

The Supreme Court recently held in *KSR Int'l Co. v. Teleflex Inc.* that "the [*Graham*] factors continue to define the inquiry that controls a finding of obviousness." 550 U.S. __, 82 USPQ2d 1385, 1397 (2007). The *Graham* factors include determining the scope and content of the prior art, ascertaining differences between the prior art and the claims at issue, and resolving the level of ordinary skill in the pertinent art. *Graham v. John Deere*, 383 U.S. 1, 148 USPQ 459 (1966). Applicant submits that the Office Action has not properly shown that the claims would have been obvious by conducting an examination of the *Graham* factors. "Patent examiners carry

the responsibility of making sure that the standard of patentability enunciated by the Supreme Court and by the Congress is applied in each and every case." *MPEP* 2141. Specifically, the Office Action has not explicitly or implicitly resolved the level of ordinary skill in the pertinent art. Therefore, the Applicant respectfully submits that the rejection is improper.

Claim 26, as amended, recites "[a] digital circuit configured as an arithmetic pipeline." According to claim 26, the circuit comprises "a flat four-input single precision floating point adder module, said module being controllable to add first, second, third and fourth single precision floating point numbers and to output a resulting single precision floating point number." The module comprises "means for predicting a largest number from exponent and mantissa portions of said floating point numbers, said predicting means outputting a plurality of shifting data calculated based on said largest number and said exponent portions; means for partially sorting said floating point numbers based on sign-bit and the exponent portions of said floating point numbers, said sorting means outputting sorted mantissas, sorted exponents, and sorted sign-bits; carry-in generation means for outputting carry-in data based on said sorted sign-bits and mantissas; addition logic receiving the carry-in data and said sorted mantissas and said plurality of shifting data, said addition logic calculating and outputting a normalized mantissa output and exponent modifier; and output logic receiving the normalized mantissa output, exponent modifier, and a largest exponent, said output logic outputting the resulting floating point number based on the normalized mantissa output, the exponent modifier, and the largest exponent."

The Office Action summarily states that Arakawa discloses "a floating point multiplier and a flat four-input floating point adder . . . includ[ing] means for predicting a largest number, carry-in generation means, negation logic[,] addition logic and output logic," but does not disclose a means for partially sorting the floating point numbers. *Office Action,* p. 4. The Office Action then states that Yoshizawa discloses means for sorting floating point numbers in a multi-input adder and that it would obvious to a person of ordinary skill in the art to "provide Arakawa with means for partially sorting the floating point numbers as taught by Yoshizawa in order to reduce the number of subtractor and aligner." *Id.* Applicant respectfully disagrees with these statements as discussed in greater detail below.

In *KSR,* the Supreme Court stated that "[r]ejections on obviousness cannot be sustained by mere conclusory statements; instead, there must be some articulated reasoning with some rational underpinning to support the legal conclusion of obviousness." *KSR*, 550 U.S. at __, 82 USPQ2d at 1396. As described in the Federal Register/Vol. 72, No. 195/Wednesday, October 10, 2007 Notices, page 57534, one rationale that may be used to show that a claim would be obvious is to show some teaching, suggestion, or motivation in the prior art that would have led one of ordinary skill to modify the prior art reference or to combine prior art reference teachings to arrive at the claimed invention. This is the rationale that the Office Action provides to hold that claim 26 is obvious. To reject a claim based on this rationale, however, the Office Action must resolve the *Graham* factual inquiries, which the Office Action has failed to do, and then articulate the following: "(1) a finding that there was some teaching, suggestion, or motivation either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings; (2) a finding that there was reasonable expectation of success; and (3) whatever additional findings based on the *Graham* factual inquiries may be necessary, in view of the facts of the case under consideration, to explain a conclusion of obviousness." *Id.*

In the case at hand, the Office Action has failed to make a *prima facie* case for obviousness at least because the Office Action has failed to articulate the findings necessary to maintain a finding of obviousness under the Office Action's chosen rationale. Specifically, the Office Action has at least failed to articulate a finding that there was a reasonable expectation of success of combining Arakawa with Yoshizawa. Applicants respectfully submit that, in fact, there was not a reasonable expectation of success for combining Arakawa with Yoshizawa, as discussed below. Therefore, the rejection of claims 26-31 is improper and the rejection should be withdrawn.

First, Arakawa does not teach all of the limitations asserted by the Office Action. The Office Action asserts that Arakawa teaches "output logic (226,227)." The limitation in claim 26, however, recites "output logic receiving the normalized mantissa output, exponent modifier, and a largest exponent, said output logic outputting the resulting floating point number based on the normalized mantissa output, the exponent modifier, and the largest exponent." The output logic

taught in Arakawa does not receive a largest exponent as an input. *Arakawa*, col. 8, lines 38-47; col. 9, lines 17-32. On the contrary, in Arakawa a largest exponent is input only into the aligner, whose output is input into the adder. *Arakawa*, col. 7, lines 53-67; col. 8, lines 1-7. As a result, this limitation of claim 26 is not taught or suggested in Arakawa because Arakawa does not teach or suggest a largest exponent as an input to either output circuit 226 or 227.

Second, even if Arakawa does teach each of the limitations asserted in the Office Action, it would not have been obvious to combine Arakawa with Yoshizawa. The limitations of claim 26 that are missing in Yoshizawa, according to the Office Action, are "means for partially sorting said floating point numbers based on sign-bit and the exponent portions of said floating point numbers, said sorting means outputting sorted mantissas, sorted exponents, and sorted sign-bits." Yoshizawa, however, teaches only sorting of exponents, not sorting of mantissas or sign bits. *Yoshizawa*, col. 14, lines 1-53. While FIG. 14 does teach a mantissa selection circuit 38, this circuit does not sort mantissas; instead, it selects the mantissa having the highest exponent. *Yoshizawa*, col. 14, lines 54-60.

Furthermore, claim 26 also recites "carry-in generation means for outputting carry-in data based on said sorted sign-bits and mantissas" and "addition logic receiving the carry-in data and said sorted mantissas and said plurality of shifting data." The limitations regarding sorted mantissas and sorted sign-bits are not taught in Arakawa and for the same reasons listed above would not be obvious in view of Yoshizawa.

As a result, claim 26 is not obvious over Arakawa in view of Yoshizawa because all limitations of claim 26 are not taught in Arakawa or Yoshizawa. Claims 27-31 depend from claim 26. Accordingly, the rejection should be withdrawn and the claims allowed.

In view of the above, Applicant believes the pending application is in condition for allowance.

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Respectfully submitted,

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